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# Analysis of the Transformerless Boost DC-DC Converter with High Voltage Gain in Different Operating Modes and Critical Inductance Calculations

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***Abstract***

*In the high voltage dc-dc boost converters, the energy transmission modes are divided into continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In addition, these modes are also divided into two different modes: complete inductor supply mode (CISM) and incomplete inductor supply mode (IISM). In this paper, the operation of the boost dc-dc converter with high voltage gain is analyzed. Firstly, the energy transmission process between CCM and DCM is analyzed. Then, this process is investigated between IISM and CISM. Moreover, the critical inductance between CCM and DCM in addition to CISM and IISM is calculated. Finally, in order to verify the presented theoretical issues, the simulation results in EMTDC/PSCAD software program are used.*

***Keywords****: Boost dc-dc converter; high voltage gain; critical inductance; energy transmission process*

## 1. Introduction

DC–DC converters are able to convert the dc input voltage level from a specific level to a desired output voltage level. The dc-dc converters could be used where the variable dc voltage sources are required. These converters are used in several applications such as distributed generation sources, power factor modification, control of the electrical machines and portable devices. The high voltage gain dc-dc converters are also used in fuel cell energy converter systems, photovoltaic energy converter systems and backup battery systems in UPS [1-6]. The boost dc-dc converter is a kind of converters that are suitable for approaching higher voltage ratings. The power switches, rectification diodes, equivalent series resistance of capacitors and inductances limit the high voltage gain. Up to now, different boost dc-dc converters have been presented in literature such as fly back ZCS-PWM [7]. The high voltage stress, which is made by the inductance leakage flux, is the main disadvantage of this converter. The transformerless boost converter is the other structure of the dc-dc converters [8]. The low size and weight are two main advantages of this converter in comparison with the converters including transformer. This converter consists of the simple structure but it includes of several disadvantages. In this converter, when the switches are turned on three power devices conduct while the switches are turned off two of power devices conduct. The high voltage stress of power switches is the other disadvantages of this converter that is equal to the output voltage.

A new converter that has been presented in [9] consists of simpler structure and lower cost. In this converter, when the switches are turned on two power devices conduct while the switches are turned off a power device conduct. In addition, the switching losses and voltage stress on the power switches are lower than the output voltage. Moreover, the amount of the current stress is same the previous structure. The voltage stress on active switches are selected based on the value of the nominal voltage and small resistance level when are turned on. In the high voltage boost dc-dc converters, the energy transmission modes are divided into CCM and DCM. The CCM is divided into CISM and IISM. In CISM, the minimum value of the inductance current is higher than the output current. In other word, the dc source not only supplies the output current but also provides the required current for charging the capacitor. In IISM, the

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minimum current value of each inductance is lower than the load current. There is no CISM in DCM and the converter is only operates in IISM.

In this paper, first the energy transmission process in CCM and DCM of the presented topology in [9] is analyzed and then this process between CISM and IISM is investigated. In addition, the voltage gain is calculated in CCM and DCM. Then, the value critical inductance between CCM and DCM in addition to CISM and IISM is calculated. Finally, the accuracy of the theoretical issues is reconfirmed through the simulation results.

## 2. The Energy Transmission Process in CCM and DCM

Figure 1 shows the high voltage boost dc-dc converter that has been presented in [9]. The converter that is shown in Figure 1 consists of two different CCM and DCM as same as conventional dc-dc converters. The operating modes in a dc-dc converter could be divided based on the values of the input voltage, duty cycle and inductance of the converter. In this paper, the operating modes of the converter are determined based on the value of the inductance. By comparing the load current and the minimum current of the inductances $L_1$ and $L_2$, the CCM is divided into CISM and IISM modes. The differences between these two modes are determined by the value of the critical inductance.

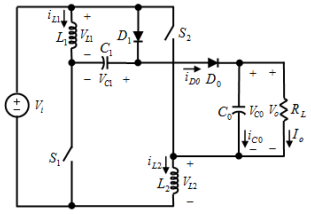


Figure 1. The boost dc-dc converter presented in [9]

### 2.1. Energy Transmission Process in CCM

In CCM the current of inductance is existed continuously in all time. The energy transmission process in CCM based on the minimum value of the inductance current $(I_{LV})$ and load current $(I_o)$ is divided into two main groups; CISM when $I_{LV} > I_o$ and IISM when $I_{LV} < I_o$.

#### 1). Complete Inductor Supply Mode (CISM)

In CISM, the minimum value of each inductor current is higher than the value of the load current. The energy transmission process is analyzed into two time intervals. The first one is the time that the switch is turned on ($T_{on}$) and the second one while the switch is turned off ($T_{off}$). In the time interval of $T_{on}$, by turning on the switches $S_1$ and $S_2$, the diodes of $D_0$ and $D_1$ are in reveres and direct connection, respectively. Figure 2(a) indicates this state. It is pointed out that the values of the inductances are considered equal. As shown in Figure 2(a), the voltages of the inductances $L_1$ and $L_2$ are equal to each other that are equal to the input voltage. In addition, by turning on the switches, the current of the inductances $L_1$ and $L_2$ are linearly increased to their maximum values that are indicated in Figure 3(a). In this time interval, according to the state of $D_0$, the capacitor $C_0$ supplies the load energy lonely that leads to reduce the voltage of the capacitor from maximum to its minimum value linearly. In addition, because of the parallel connection of the capacitor $C_1$ and input voltage $(V_i)$, this capacitor is charged to $V_i$. In the time interval of $T_{off}$, by turning off the switches $S_1$ and $S_2$, the diodes $D_0$ and $D_1$ are in direct and reveres connection, respectively. Figure 2(b) indicates this state. As shown in Figure 2(b), the inductances $L_1$ and $L_2$ are connected in series and so their current are equal to each other. Therefore, the current of the inductances are considered $i_{L1} = i_{L2} = i_L$. In this time interval, the inductance supplies the load and capacitor and so the capacitor is charged. Therefore, by

discharging the inductance, its current is decreased from $I_{LP}$ to $I_{LV}$ that is shown in Figure 3(a). In addition, the value of the capacitor current is equal to $i_c = i_L - I_o$ therefore, the capacitor current is also reduced by decreasing the inductance current. This reduction of the capacitor current is continued until $t_3$. In the time interval of $(t_1 - t_3)$, the value of the capacitor voltage is increased from $V_{cv}$ to $V_{cp}$ that is equal to its maximum value. In addition, the voltage of the capacitor $C_1$ is constant and equal to $V_i$ because the capacitance value of $C_1$ is considered high enough.

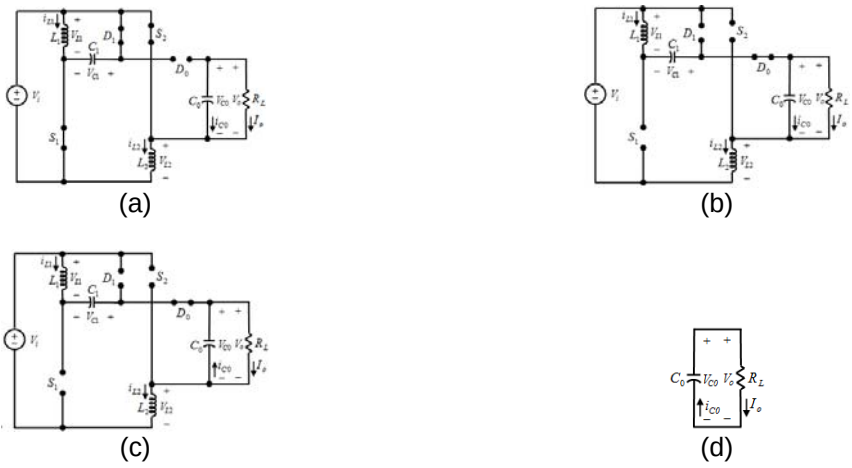


Figure 2. The operating mods of the converter; (a) $T_{on}$; (b) $T_{off}$ while $i_L > I_o$; (c) $T_{off}$ while $i_L < I_o$; (d) $T_{off}$ while $i_L = 0$

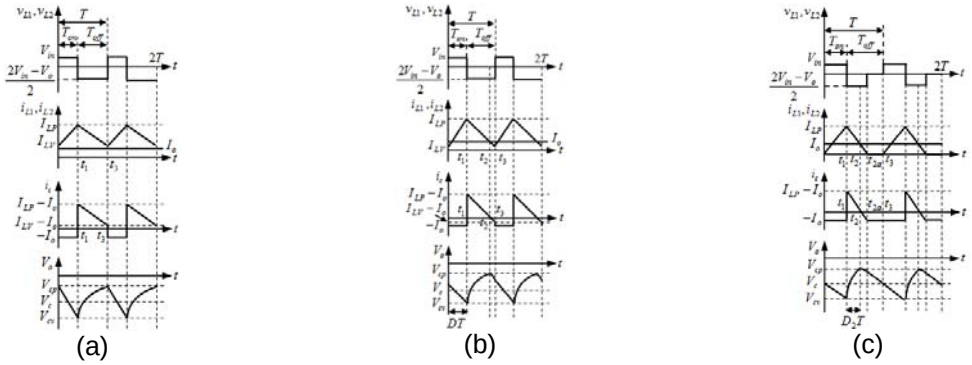


Figure 3. Voltage and current waveforms; (a) CISM-CCM; (b) IISM-CCM; (c) IISM-DCM

**2). Incomplete Inductor Supply Mode (IISM)**

In IISM, the minimum value of each inductor current is lower than the value of the load current. The analysis of this operating mode is as same as CISM and is divided into two time interval of $T_{on}$ and $T_{off}$. The waveforms of the inductances voltage, inductances current, capacitor current and output voltage in IISM are shown in Figure 3(b). The analysis of the converter in the time interval of $T_{on}$ is as same as CISM by the differences that the primary value of the inductance current and output voltage in IISM is differ from CISM. The energy transmission process in the time interval of $T_{off}$ is divided into two states.

**First state:** This state consists of the time interval of $(t_1 - t_2)$. As shown in Figure 2(b), in this time interval, the inductance current supplies the load current and charges the capacitor. Therefore, by decreasing the inductance current based on the equation $i_c = i_L - I_o$, the

capacitor current of $C_0$ is also reduced. At $t_2$, the capacitor current of $C_0$ will be equal to zero when the inductance current is equal to load current.

**Second state:** This state consists of the time interval of $(t_2 - t_3)$. In IISM mode and in the time interval of $(t_2 - t_3)$, by decreasing the inductance current, the capacitor current of $C_0$ is also reduced based on the equation of $i_c = i_L - I_o$ until $t_3$ that its value will be equal to $I_{LV} - I_o$ because the minimum value of the inductance current is lower than the load current. This state is shown in Figure 2(c). As shown in Figure 2(c) and in the time interval of $(t_2 - t_3)$, the capacitor voltage of $C_0$ is reduced by discharging the energy of the capacitor.

### 2.2. Energy Transmission Process in DCM

In DCM, the value of the inductance current is equal to zero in a time interval and is apposite of zero in another time interval. Therefore, the value of the inductance current is lower than the value of the load current. As a result, there is no CISM in DCM and the converter operates only in IISM. In DCM, the waveforms of the inductances voltage, inductances current, capacitor current of $C_0$ and output voltage are shown in Figure 3. As same as CCM, the operating of the converter in DCM is investigated into two time intervals $T_{on}$ and $T_{off}$. The energy transmission process is as same as CCM when the switches are turned on. The operating analysis of the converter in the time interval of $T_{off}$ is divided into three time intervals as follows:

**First state:** This state consists of the time interval of $(t_1 - t_2)$. This state is indicated in Figure 2(b). As shown in this figure, the inductance supplies the load current in addition to charge the capacitor, therefore, by discharging the inductances, their current are reduced and so the capacitors current are also decreased based on the equation $i_c = i_L - I_o$. In $t_2$, the capacitor current will be equal to zero when the inductance current is equal to the load current. At this time interval, the capacitor voltage is also increased because it is charged.

**Second state:** This state consists of the time interval of $(t_2 - t_{2a})$. In this time interval, by decreasing the inductance current, the capacitor current of $C_0$ is also reduced based on the equation $i_c = i_L - I_o$. This state is indicated in Figure 2(c). As shown in Figure 2(c), the inductances and the capacitor of $C_0$ supply the load energy because in this time interval the minimum value of inductances current are lower than the load current as same as IISM-CCM. At $t_{2a}$, the current of the capacitor $C_0$ will be equal to $(-I_o)$ because the inductances current are equal to zero.

**Third state:** This state consists of the time interval of $(t_{2a} - t_3)$. In this time interval, the capacitor $C_0$ only supplies the load energy because the values of the inductances current are equal to zero. This state is indicated in Figure 2(d). As shown in Figure 2(d), the current of the capacitor $C_0$ is equal to $(-I_o)$ and by discharging the capacitor $C_0$, its voltage is linearly reduced**.**

## 3. Voltage Gain Calculation in CCM and DCM

The voltage gain is one of the most important parameters in analysis of the dc-dc converters that indicates the relation between output and input voltage. The voltage gain of the converter is written based on the duty cycle of the converter and other parameters of the converter. For the converter shown in Figure 1, the value of the inductances $L_1$ and $L_2$ are considered equally and are shown by $L$. The duty cycle of the converter is written as follows:

$$D = \frac{T_{on}}{T} \tag{1}$$

It is resulted from above equation that:

$$1-D=\frac{T_{off}}{T} \tag{2}$$

### 3.1. Voltage Gain in CCM

The voltage gain in CCM is obtained from the voltage balance law of the inductance as follows:

$$\frac{1}{T}\int_0^T v_L(t)dt=0 \tag{3}$$

According to Figure 2(a) and based on the Kirchhoff voltage law, the voltage magnitude of each inductance in the time interval of $T_{on}$ is equal to:

$$v_{L1}=v_{L2}=v_L=V_{in} \tag{4}$$

In this time interval, because of the same value of the inductances it could be written:

$$i_{L1}=i_{L2}=i_L \tag{5}$$

In the time interval of $T_{off}$ as shown on Figure 2(b), the equation (5) is valid because the series connection of the inductances. By using the Kirchhoff voltage law in the shown circuit in Figure 2(b) and based on the magnitude of the capacitor voltage that is equal to $V_i$, the below equation is written:

$$v_{L1}=v_{L2}=v_L=\frac{2V_i-V_o}{2} \tag{6}$$

Based on equation (1) and by considering $T=T_{on}+T_{off}$, the (3) is rewritten as follows:

$$\frac{1}{T}\left[\int_0^{DT} v_L(t)dt+\int_0^{(1-D)T} v_L(t)dt+\right]=0 \tag{7}$$

By replacing (4) and (6) into (7), the voltage gain in CCM is calculated a follows:

$$\frac{V_o}{V_i}=\frac{2}{1-D} \tag{8}$$

### 3.2. Voltage Gain in DCM

The voltage gain in DCM is obtained from the current balance law of the capacitor as follows:

$$\frac{1}{T}\int_0^T i_{c_0}(t)=0 \tag{9}$$

According to Figure 3 and in the time interval of $T_{on}$, the capacitor current is equal to $(-I_o)$. As shown in this figure, the time interval $T_{off}$ is divide into two time intervals $(t_1-t_{2a})$ and $(t_{2a}-t_3)$. In the time of $(t_1-t_{2a})$, by assuming $t_1=0$ (the new time offset ) the capacitor current will be equal to:

$$i_{c_0}(t)=\frac{2V_i-V_o}{2L}t+I_{LP}-I_o \tag{10}$$

In (10), the $I_{LP}$ is the maximum value of the inductance current and the primary value of the inductance current in $(t_1 - t_3)$. According to Figure 3, the current value of the capacitor $C_0$ in the time interval of $(t_{2a} - t_3)$ is equal to $(-I_o)$. By considering $(t_{2a} - t_1 = D_2 T)$ and based on (1), (9) could be rewritten as follows:

$$\frac{1}{T}\left[\int_0^{T_{on}} i_{c_0}(t)dt + \int_0^{D_2 T} i_{c_0}(t)dt + \int_0^{(1-D-D_2)T} i_{c_0}(t)dt\right] = 0 \quad (11)$$

Therefore, the maximum value of the inductances current is calculated as follows:

$$I_{LP} = \frac{V_i D}{Lf} \quad (12)$$

when $f$ is the switching frequency.
According to the facts that the average value of the inductance voltage in a switching period is equal to zero, in DCM, the value of $D_2$ is calculated as follows:

$$D_2 = \frac{2DV_i}{V_o - 2V_i} \quad (13)$$

In DCM, the voltage gain is equal to:

$$\frac{V_o}{V_i} = 1 + \sqrt{1 + \frac{D^2 R_L}{Lf}} \quad (14)$$

## 4. Calculation of Critical Inductance

It is pointed out that the operating modes of the converter are determined based on the value of the inductances current and this value is depends on the value of the inductances. Therefore, in order to calculate the critical inductance between different operating modes, the equations of the inductances current have to be calculated.

### 4.1. Critical Inductance Calculation between CCM and DCM

The minimum value of the inductance current between CCM and DCM is equal to zero. Therefore, the value of the critical inductance between CCM and DCM is obtained by calculation the value of $I_{LV}$ versus the inductance while it is equalized to zero. In the time interval $(0 - t_1)$, the inductance current is obtained as follows:

$$i_L(t) = \frac{V_i}{L}t + I_{LV} \quad (15)$$

By replacing the margin conditions in (15), it is resulted:

$$I_{LP} = \frac{V_i}{L}t + I_{LV} \quad (16)$$

The value of the $I_{LP}$ is obtained based on the capacitor current balance law as follows:

$$\frac{1}{T}\int_0^T i_{c_0}(t)dt = 0 \quad (17)$$

As shown in Figure 3, (17) is divided into two time intervals of $T_{on}$ and $T_{off}$ . In the time interval of $T_{on}$ , the current value of the capacitor $C_0$ is equal to $-I_o$ and at the time interval of $T_{off}$ by assuming $t_1 = 0$ it is equal to:

$$i_{c_0}(t) = i_L(t) - I_o \tag{18}$$

In (18), $i_L(t)$ is the current of each inductance in the time interval of $T_{off}$ . By considering $t_1 = 0$ as the new time offset and by solving (18), the value of the inductance current in the time interval of $T_{off}$ is calculated as follows:

$$i_L(t) = \frac{2V_i - V_o}{2L}t + I_{LP} \tag{19}$$

By replacing (19) into (18) and (17), the maximum and the minimum value of the inductance current are obtained as follows:

$$I_{LP} = I_o\left[\frac{1}{1-D} + \frac{R_L D(1-D)}{4Lf}\right] \tag{20}$$

$$I_{LV} = I_o\left[\frac{1}{1-D} - \frac{R_L D(1-D)}{4Lf}\right] \tag{21}$$

The value of the critical inductance is obtained when $I_{LV} = 0$ as follows:

$$L_C = \frac{R_L D(1-D)^2}{4f} = \frac{R_L V_i^2 (V_o - 2V_i)}{f V_o^3} \tag{22}$$

The converter is in CCM when $L > L_C$ and is in DCM while $L < L_C$ .

### 4.2. Calculation of Critical Inductance between CISM and IISM

The minimum value of the inductance current between CISM and IISM is equal to the load current. Therefore, the critical inductance between CISM and IISM are equal to:

$$L_K = \frac{R_L(1-D)^2}{4f} = \frac{R_L V_i^2}{f V_o^2} \tag{23}$$

The converter is in CISM when $L > L_K$ and is in IISM while $L < L_K$ . Therefore:

$$L_K = \frac{L_C}{D} \tag{24}$$

By considering $0 < D < 1$, it is resulted that $L_K > L_C$. Therefore, the operating modes of converter could be divided into three different modes. These divisions are shown in Figure 4. As shown in this figure, the operating modes are as follows:

CISM-CCM: in this mode $L > L_K$ and $I_{LV} > I_o$

IISM-CCM: in this mode $L_C < L < L_K$ and $I_{LV} < I_o$

IISM-DCM: in this mode $L < L_C$ and $I_{LV} < I_o$

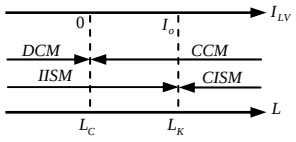


Figure 4. The operating modes versus $I_{LV}$ and $L$

For a dc-dc converter in the different operating conditions, the values of the input voltage and load resistance could be changed between two minimum and maximum values. Based on (22) and (23), it is clear that the values of $L_C$ and $L_K$ are depends on the values of the input voltage and load resistance. The value of $V_i$ could be changed between $V_{i,\min}$ to $V_{i,\max}$ and the value of load resistance between $R_{L,\min}$ to $R_{L,\max}$. Therefore, the operating region of the converter is a rectangular (ABCD) in the page of $R_L - V_i$ as shown in Figure 5. By changing the values of $V_i$ and $R_L$, the values of $L_C$ and $L_K$ are changed that lead to change the operating mode of the converter versus a specific value of the inductance. Figures 5(a) and 5(b) show the operating region of the converter in different operating modes versus $L_C$ and $L_K$ in the page of $R_L - V_i$. It is important to note that in Figure 5, the value of $L_C$ and $L_K$ are considered $L_{C1} < L_{C,\min} < L_{C2} < L_{C,\max} < L_{C3}$ and $L_{K1} < L_{K,\min} < L_{K2} < L_{K,\max} < L_{K3}$.

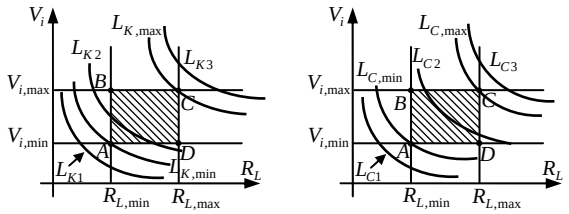


Figure 5. Different operating modes in the page of $R_L - V_i$ ; (a) CCM and DCM; (b) CISM and IISM

It is pointed out that the points A and C in Figure 5 are the points that the minimum and maximum values of the critical inductances are obtained based on them, respectively. The minimum and maximum values of critical inductance are equal to:

$$L_{C,\min} = \frac{R_{L,\min} V_{i,\min}^2 (V_o - 2V_{i,\min})}{f V_o^3} \quad (25)$$

$$L_{C,\max} = \frac{R_{L,\max} V_{i,\max}^2 (V_o - 2V_{i,\max})}{f V_o^3} \quad (26)$$

$$L_{K,\min} = \frac{R_{L,\min} V_{i,\min}^2}{f V_o^2} \quad (27)$$

$$L_{K,\max} = \frac{R_{L,\max} V_{i,\max}^2}{f V_o^2} \quad (28)$$

It is obvious from Figure 5(a) that the converter is in CCM when $L > L_{C,\max}$, which is indicated by $L_{C3}$ and is in DCM while $L < L_{C,\min}$, which is indicated by $L_{C1}$ in the figure. In addition, when $L_{C,\min} < L < L_{C,\max}$, according to $V_{i,\min} < V_i < V_{i,\max}$ and $R_{L,\min} < R_L < R_{L,\max}$, by considering the specific values of $R_L$ and $V_i$, the converter will be in CCM when $L > L_C$ and will be in DCM while $L < L_C$, which is shown by $L_{C2}$ in Figure 5(a). Moreover, if $L > L_{K,\max}$, the converter is in CISM which is indicated by $L_{K3}$ and if $L < L_{K,\min}$, the converter will be in IISM, which is indicated by $L_{K1}$ in Figure 5(b). For the states that $L_{\mathrm{K,min}} < L < L_{\mathrm{K,max}}$, according to $V_{i,\min} < V_i < V_{i,\max}$, $R_{L,\min} < R_L < R_{L,\max}$ and based on considering the specific value of $R_L$ and $V_i$, the converter is in CISM when $L > L_K$ and will be in IISM while $L < L_K$, which is indicated by $L_{K2}$ in Figure 5(b).

## 5. Simulation Results

The correct performance of the presented high voltage dc-dc converter that is shown in Figure 1 is verified through simulation results in different operating modes. The simulation results are obtained by EMTDC/PSCAD software program. The values of the main parameters of the converter are summarized in Table I. Considering (25) to (28) and Table I, the values of the inductances and capacitance are obtained as shown in Table II.

Table 1. The Main Parameter of The Converter

| Parameters | Values |
|---|---|
| $f$ | $kHz$ 100 |
| $V_i$ | $10V - 14V$ |
| $R_L$ | $90\Omega - 250\Omega$ |
| $V_o$ | $45V$ |
| $C_1$ | $50\,\mu F$ |

Table 2. The Value of The Inductances and Capacitance of Converter

| | |
|---|---|
| $L_{C,\min}$ | $21.6\,\mu H$ |
| $L_{C,\max}$ | $86.24\,\mu H$ |
| $L_{K,\min}$ | $36\,\mu H$ |
| $L_{K,\max}$ | $196\,mH$ |

According to Table I, the values of input voltage and load resistance are selected $V_i = 12V$ and $R_L = 150\Omega$, respectively. By replacing these values in (22) and (23), the critical inductances are equal to $L_C = 44.93\mu H$ and $L_K = 86.4\mu H$.

Figure 6 shows the output voltage and inductance current waveforms versus different values of inductances. As shown in Figure 6(a), by considering $L = 25\mu H$, the converter is in IISM-DCM because this value is lower than the critical inductance ($L_C = 44.93\mu H$). In addition, if the value of the inductance is selected $L = 70\mu H$, the converter is in IISM-CCM because the selected value is between $L_C = 44.93\mu H$ and $L_K = 86.4\mu H$ (Figure 6(b)). When the value of the inductance is selected $L = 95\mu H$, the converter is in CISM-CCM because the selected value is higher than $L_K = 86.4\mu H$ (Figure 6(c)). As it is obvious from Figure 6, the simulation results reconfirm the shown waveforms in Figure 3.

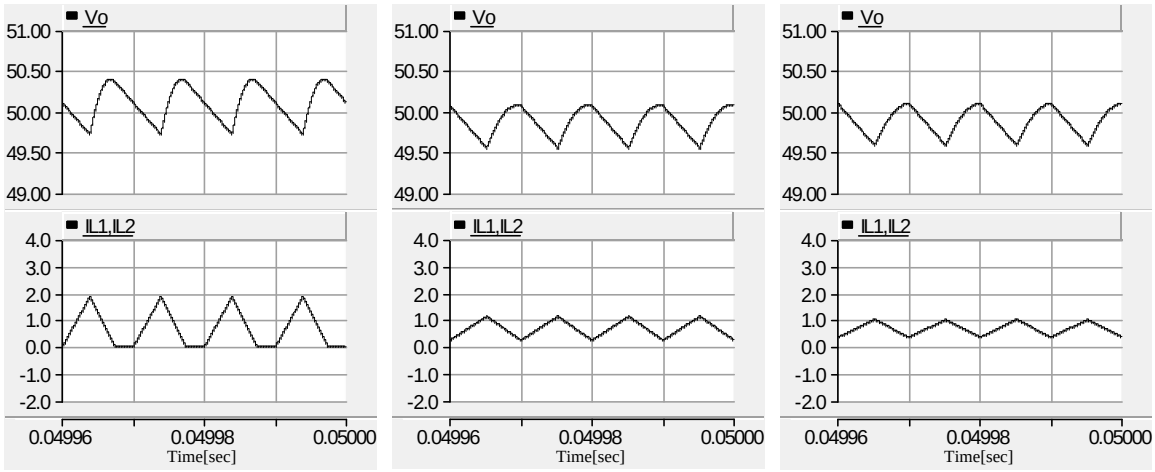


Figure 6. The simulation results of the converter in different operating modes; (a) IISM-DCM; (b) IISM-CCM; (c) CISM-CCM

## 6. Conclusion

In this paper, the transformerless boost dc-dc converter with high voltage gain that is presented in [9] is analyzed. The mathematical equations for different operating modes are calculated. The different operating modes in dc-dc converter are determined by the value of the inductance. By comparing the minimum value of inductance current and load current the CCM is divided into two modes CISM and IISM that the border of these two modes are determined by the value of the critical inductance. There is no CISM in DCM and the converter is only operates in IISM. In other words, the operating modes of the high voltage boost dc-dc converter are divided into three operating modes: CISM-CCM, IISM-CCM, and IISM-DCM. In CISM, the minimum current value of each inductance is higher than the load current and in IISM the minimum current value of each inductance is lower than the load current. For the high voltage boost dc-dc converter in different operating modes, the values of the input voltage and load resistance could be changed between two minimum and maximum values and the value of the critical inductances is depends on the value of the input voltage and load current. Finally, the accuracy performance of the theoretical issues is reconfirmed by the simulation results in EMTDC/PSCAD software program.

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